CLAIMS:

1. A hardware-based multi-bit halftoning system for use with a marking engine, the system comprising:

a raster-data obtainer circuitry configured to obtain raster data, the data including pixels and their grayscale values;

a threshold memory configured to store a matrix of threshold values;

a comparator circuitry configured to concurrently compare the threshold values of multiple entries in the matrix to the grayscale values of corresponding multiple pixels of the raster data.

2. A system as recited in claim 1, further comprising:

a scale resolver circuitry configured to receive raster data from the obtainer circuitry and converts resolution scale of raster data to a specified resolution scale of a marking engine;

a halftone-cell address calculator circuitry configured to translate addresses of the scaled raster data into threshold addresses.

3. A system as recited in claim 1, wherein the threshold values have a halftone-depth and the grayscale data has a grayscale-depth.

4. A system as recited in claim 1, wherein the threshold values have a halftone-depth and the grayscale data has a grayscale-depth and wherein the grayscale-depth does not match the halftone-depth.

5. A system as recited in claim 1 further comprising a threshold loader circuitry configured to load the threshold memory with the matrix, wherein the resolution of the loaded matrix matches the resolution of the raster data.

6. A system as recited in claim 1 further comprising a threshold loader circuitry configured to load the threshold memory with the matrix, wherein the threshold values have a halftone-depth and the grayscale data has a grayscale-depth and wherein the grayscale-depth does not match the halftone-depth.

7. A system as recited in claim 1 further comprising a decoder circuitry configured to decode the comparisons of the comparator circuitry to generate an index of pixel locations of the raster data where the grayscale data is between adjacent threshold values.

8. A system as recited in claim 1, wherein threshold matrix forms a dithering pattern.

9. A system as recited in claim 1, wherein the hardware-based memory management system is embodied as, at least part of, an application specific integrated circuit (ASIC).

10. A hardware-based multi-bit halftoning system for use with a marking engine, the system comprising:

a raster-data obtainer circuitry configured to obtain raster data, the data including pixels and their grayscale values;

a threshold memory configured to store a matrix of threshold values;

a comparator circuitry configured to compare threshold values of the matrix to grayscale values of corresponding pixels of the raster data.

11. A system as recited in claim 10, wherein the comparator circuitry is further configured to concurrently compare the threshold values of multiple entries in the matrix to the grayscale values of corresponding multiple pixels of the raster data.

12. A system as recited in claim 10, wherein the threshold values have a halftone-depth and the grayscale data has a grayscale-depth and wherein the grayscale-depth does not match the halftone-depth.

13. A system as recited in claim 10 further comprising a threshold loader circuitry configured to load the threshold memory with the matrix, wherein the resolution of the loaded matrix matches the resolution of the raster data.

14. A system as recited in claim 10 further comprising a threshold loader circuitry configured to load the threshold memory with the matrix, wherein the threshold values have a halftone-depth and the grayscale data has a grayscale-depth and wherein the grayscale-depth does not match the halftone-depth.

15. A system as recited in claim 10 further comprising a decoder circuitry configured to decode the comparisons of the comparator circuitry to generate an index of pixel locations of the raster data where the grayscale data is between adjacent threshold values.

16. A system as recited in claim 10, wherein threshold matrix forms a dithering pattern.

17. A system as recited in claim 10, wherein the hardware-based memory management system is embodied as, at least part of, an application specific integrated circuit (ASIC).

18. With a hardware-based multi-bit halftoning module configured to flexibly and efficiently halftone raster data containing a continuous tone image, a method comprising:

setting halftone-depth and resolution of threshold matrix;

obtaining raster data, the data including pixels and their grayscale values;

loading the threshold matrix with threshold values;

comparing thresholds in the matrix to the grayscale data of corresponding pixels of the raster data.

19. A method as recited claim 18, wherein during the comparing, the threshold values of multiple entries in the matrix are concurrently compared the grayscale values of corresponding multiple pixels of the raster data.

20. A method as recited claim 18, wherein the threshold values have a halftone-depth and the grayscale data has a grayscale-depth and wherein the grayscale-depth does not match the halftone-depth.

21. A method as recited claim 18 further comprising decoding the results of the comparing to generate an index of pixel locations of the raster data where the grayscale data is between adjacent threshold values.